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[Title Of The Invention]
SEMICONDUCTOR DEVICE

[Abstract]
PROBLEM TO BE SOLVED: To obtain a large electrostatic capacity and absorbing high frequency noise in a wide band, by forming a capacitor wherein dielectrics is sandwiched between two electrodes on a board on which an IC die is mounted, and connecting the respective electrodes of the capacitor to a power supply pad and a ground pad of the IC die.
SOLUTION: A capacitor formed by sandwiching dielectrics 32 by a first and a second plane type conductors 30, 31 is arranged on a board 25 having a plurality of signal I/O terminals 27, a power supply terminal 28, a ground terminal 29 and a wiring pattern 35. An IC die 26 having a plurality of bonding pads 26-1 for signal input and output, a bonding pad 26-2 for a power supply, and a bonding pad 26-3 for ground is surface-mounted on the board 25. The power supply terminal 28 is connected to a terminal 30-1 of the first plane type conductor 30 and the bonding pad 26-2 for the power supply of the IC die 26. The bonding pad 26-3 for ground of the IC die 26 and a terminal 31-1 of the second plane type conductor 31 are connected to the ground terminal 29.

[Claim(s)]
[Claim 1]A substrate which has two or more signal input/output terminals, at least one power supply terminal, and at least one earthing terminal, At least one IC die which has two or more bonding pads for signal input and output and at least one bonding pad for power supplies which were connected to a circuit pattern which surface mounting was carried out to this substrate, and was provided in the above-mentioned substrate, respectively, and at least one bonding pad for grounding, It has a capacitor which was formed on both sides of a dielectric with at least one first and the second surface state conductor, and was allocated by the above-mentioned substrate, A semiconductor device which said first and the second surface state conductor provided a terminal in a part of surface state, respectively, connected a bonding pad for power supplies of said IC die with said power supply terminal and a terminal of said first surface state conductor, and connected a bonding pad for grounding of said IC die, a terminal of the second [said] surface state conductor, and said earthing terminal.
[Claim 2]At least one IC die by which a bonding pad was connected to a substrate provided with two or more through holes which flow through substrate both sides, and a circuit pattern which surface mounting was carried out to one field of this substrate, and was provided in the above-mentioned substrate, respectively, Two or more signal input/output terminals and at least one power supply terminal which were provided in a field of another side of this board, and at least one earthing terminal, It is allocated in free space of this terminal and the above-mentioned substrate except a through hole, and has a capacitor formed on both sides of a dielectric with at least one first and the second surface state conductor, A power supply terminal which said first and the second surface state

conductor provided a terminal in a part of surface state, respectively, and was provided in this substrate connects a through hole established in the first terminal and said substrate of a surface state conductor, A circuit pattern linked to a bonding pad for power supplies of this through hole and said IC die is connected, A semiconductor device which connected a circuit pattern which an earthing terminal formed in this board connects a through hole established in the second terminal and said substrate of a surface state conductor, and is connected to a bonding pad for grounding of this through hole and said IC die.

[Claim 3]On both sides of a dielectric, it is formed in one field of a substrate provided with two or more through holes which flow through substrate both sides, and this substrate in free space except said through hole with at least one first and the second surface state conductor, A capacitor which provided a terminal, respectively in a part of surface state of said first and the second surface state conductor, Two or more signal input/output terminals and at least one power supply terminal which were provided in a field of another side of this board, and at least one earthing terminal, It is mounted in a field of another side of the above-mentioned substrate, and has at least one IC die connected to a circuit pattern linked to a bonding pad provided in a field of another side of the above-mentioned substrate, A power supply terminal provided in this board is connected with a terminal of the first surface state conductor of said capacitor via a circuit pattern linked to a bonding pad for power supplies of said IC die, and a through hole established in said substrate, A semiconductor device connected with a terminal of the second surface state conductor of said capacitor via a circuit pattern which connects to a bonding pad for grounding of said IC die an earthing terminal formed in this substrate, and a through hole established in said substrate.

[Claim 4]The semiconductor device according to any one of claims 1 to 3 having arranged a signal input/output terminal and a power supply terminal which were provided in a substrate, and an earthing terminal in the shape of a lattice by a spherical shape, respectively.

[Claim 5]The semiconductor device according to any one of claims 1 to 3 having arranged a signal input/output terminal and a power supply terminal which were provided in a substrate, and an earthing terminal in the shape of a lattice with pin geometry, respectively.

[Claim 6]The semiconductor device according to any one of claims 1 to 3 forming a capacitor in a substrate by printing.

[Claim 7]It has a TAB package mounted in this at least one opening of a carrier film which has an opening for an IC die characterized by comprising the following, The second signal input/output terminal provided in this carrier film is connected to a bonding pad for signal input and output of said IC die, The second power supply terminal provided in this carrier film is connected to a bonding pad for power supplies of said IC die, A semiconductor device which connected to a bonding pad for grounding of said IC die the second earthing terminal formed in this carrier film, connected with a terminal of said first surface state conductor the third power supply terminal provided in this carrier film, and connected the third earthing terminal with a terminal of said second surface state conductor.

A substrate.

At least one capacitor which it was allocated on this substrate and formed in a part of surface state on both sides of a dielectric with the first which has a terminal, respectively, and the second surface state conductor.

It is arranged in piles on this capacitor, A circuit pattern and first at least one power supply

terminal which connect two or more first signal input/output terminals, two or more second signal input/output terminals, this first, and the second signal input/output terminal, second at least one power supply terminal, third at least one power supply terminal, this first, and the second and the third power supply terminal. It has a circuit pattern which connects a circuit pattern and first at least one earthing terminal to connect, second at least one earthing terminal, third at least one earthing terminal, this first, and the second and the third earthing terminal, Two or more bonding pads for signal input and output, at least one bonding pad for power supplies, and at least one bonding pad for grounding.

[Claim 8]The semiconductor device according to claim 7 which made plate shape the first signal input/output terminal, first power supply terminal, and first earthing terminal, respectively.

[Claim 9]The semiconductor device according to claim 7 which has arranged the first signal input/output terminal, first power supply terminal, and first earthing terminal in the shape of a lattice by a spherical shape, respectively.

[Claim 10]The semiconductor device according to claim 7 which has arranged the first signal input/output terminal, first power supply terminal, and first earthing terminal in the shape of a lattice with pin geometry, respectively.

[Claim 11]It has a TAB package mounted in this at least one opening of a carrier film which has an opening for an IC die characterized by comprising the following, The second signal input/output terminal provided in this carrier film is connected to a bonding pad for signal input and output of said IC die, The second power supply terminal provided in this carrier film is connected to a bonding pad for power supplies of said IC die, The second earthing terminal formed in this carrier film is connected to a bonding pad for grounding of said IC die, A semiconductor device arranged on both sides of a capacitor which connected with a terminal of said first surface state conductor the third power supply terminal provided in this carrier film, connected the third earthing terminal with a terminal of said second surface state conductor, and was allocated in said substrate with said back up plate and said TAB package.

A substrate reinforced by the back up plate.

At least one capacitor which it was allocated on this substrate and formed in a part of surface state on both sides of a dielectric with the first which has a terminal, respectively, and the second surface state conductor.

It is arranged in piles on this capacitor, A circuit pattern and first at least one power supply terminal which connect two or more first signal input/output terminals, two or more second signal input/output terminals, this first, and the second signal input/output terminal, second at least one power supply terminal, third at least one power supply terminal, this first, and the second and the third power supply terminal. It has a circuit pattern which connects a circuit pattern and first at least one earthing terminal to connect, second at least one earthing terminal, third at least one earthing terminal, this first, and the second and the third earthing terminal, Two or more bonding pads for signal input and output, at least one bonding pad for power supplies, and at least one bonding pad for grounding.

[Claim 12]The semiconductor device according to claim 11 which used the back up plate as metal.

[Claim 13]The semiconductor device according to claim 11 which carried out alumite treatment of the surface of this aluminum while making the back up plate into aluminum.

[Claim 14]The semiconductor device according to claim 11 which formed a capacitor in

the back up plate by printing.

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the semiconductor device having capacitors, such as a microprocessor which carries out high-speed operation.
[0002]
[Description of the Prior Art]Drawing 6 is a perspective view of the conventional pin grid array form ceramic package for high-speed microprocessors. In drawing 6, 1 is a terminal, 2 is the package base which arranged the terminal 1 in the shape of a lattice, 3 is a laminated ceramic capacitor (it is henceforth called a chip capacitor) of a surface mounting type, and 4 is a radiator. Although not illustrated by drawing 6, it is built in the package base 2, and is connected to the terminal 1 arranged in the shape of a lattice, and the die of a microprocessor has cooled generation of heat at the time of operation with the radiator 4. The terminal of the two poles of the chip capacitor 3 mounted in the package base 2 is connected also to the terminal 1 while being connected to at least one power supply terminal and earthing terminal of a microprocessor, respectively.
[0003]Drawing 7 is a sectional view of a semiconductor device given in JP,63-239970,A. In drawing 7, 5 is a die of IC, 6 is a circuit formation side of IC, 7 is the power supply wiring inside a die, and 8 is the grounding wiring inside a die. 9 and 10 are polyimide system resin layers, 11, 12, and 13 are through holes, 14 and 15 are electrode metal layers, 16 is a metal layer, and 17, 18, and 19 are terminal areas. It is what formed the capacitor which the electrode metal layers 14 and 15 were made to counter via the polyimide system resin layer 10 on the circuit formation side 6 of IC via the insulating layer of the polyimide system resin layer 9, The electrode metal layer 14 is the capacitor which connected the electrode metal layer 15 to the power supply wiring 7 inside a die via the terminal areas 18 and 19 at the grounding wiring 8 inside a die via the terminal area 17, respectively.
[0004]
[Problem(s) to be Solved by the Invention]In order to accelerate a computer, while accelerating a bus clock, internal clock frequency of a microprocessor is usually made high. In this case, the power consumption of the microprocessor increased and it had a problem of a high frequency noise being overlapped on power supply voltage, and making a microprocessor for a microprocessor to not only be to overheat, but malfunction.
[0005]Therefore, the method of mounting many chip capacitors in a package base like drawing 6 conventionally, or forming a capacitor on the circuit formation side 6 of an IC die like drawing 7 is proposed. However, in the case of drawing 6, the complicated man day which mounts many chip capacitors started, and when it was drawing 7, there was a problem that the electrostatic capacity value of a capacitor was restrained by the size of an IC die.
[0006]This invention solves such a conventional problem.
The purpose is to provide the semiconductor device which large electric capacity is obtained and can absorb a broad high frequency noise.
[0007]
[Means for Solving the Problem]In order to solve the above-mentioned technical problem, a semiconductor device of this invention forms at least two or more capacitors which inserted a dielectric into a substrate with which an IC die is mounted by two electrodes,

and connects each electrode of each of this capacitor to a power supply pad and a ground pad of an IC die, respectively. Therefore, since it can constitute from a broad electrode area, big electric capacity is obtained, and this capacitor functions as a bypass capacitor which absorbs a broad high frequency noise.

[0008]

[Embodiment of the Invention]The substrate with which the invention of this invention according to claim 1 has two or more signal input/output terminals, at least one power supply terminal, and at least one earthing terminal, At least one IC die which has two or more bonding pads for signal input and output and at least one bonding pad for power supplies which were connected to the circuit pattern which surface mounting was carried out to this substrate, and was provided in the above-mentioned substrate, respectively, and at least one bonding pad for grounding, It has the capacitor which was formed on both sides of the dielectric with at least one first and the second surface state conductor, and was allocated by the above-mentioned substrate, Said first and the second surface state conductor provide a terminal in a part of surface state, respectively, and connect the bonding pad for power supplies of said IC die with said power supply terminal and the terminal of said first surface state conductor, It is the semiconductor device which connected the bonding pad for grounding of said IC die, the terminal of said second surface state conductor, and said earthing terminal, The circuit pattern which constitutes a capacitor from piling up on both sides of a dielectric with a surface state conductor, and connects the bonding pad for power supplies of an IC die with a power supply terminal for this capacitor, It has the operation of making the noise which makes arrangement connection between the circuit patterns which connect the bonding pad for grounding of an IC die with an earthing terminal, and is superimposed on power supply voltage bypass.

[0009]The substrate provided with two or more through holes where the invention of this invention according to claim 2 flows through substrate both sides, At least one IC die by which the bonding pad was connected to the circuit pattern which surface mounting was carried out to one field of this board, and was provided in the above-mentioned substrate, respectively, Two or more signal input/output terminals and at least one power supply terminal which were provided in the field of another side of this board, and at least one earthing terminal, It is allocated in the free space of this terminal and the above-mentioned substrate except a through hole, and has the capacitor formed on both sides of the dielectric with at least one first and the second surface state conductor, The power supply terminal which said first and the second surface state conductor provided the terminal in a part of surface state, respectively, and was provided in this substrate connects the through hole established in the first terminal and said substrate of the surface state conductor, The circuit pattern linked to the bonding pad for power supplies of this through hole and said IC die is connected, The earthing terminal formed in this board connects the through hole established in the second terminal and said substrate of the surface state conductor, It is the semiconductor device which connected the circuit pattern linked to the bonding pad for grounding of this through hole and said IC die, and a large surface state conductor can be formed in the rear face of the capacitor which was piled up and constituted from a surface state conductor on both sides of the dielectric by arranging an IC die, It has the operation of carrying out noise absorption with bigger electric capacity than claim 1.

[0010]The substrate provided with two or more through holes where the invention of this invention according to claim 3 flows through substrate both sides, The capacitor which

was formed in one field of this substrate on both sides of the dielectric in the free space except said through hole with at least one first and the second surface state conductor, and provided the terminal, respectively in a part of surface state of said first and the second surface state conductor, Two or more signal input/output terminals and at least one power supply terminal which were provided in the field of another side of this board, and at least one earthing terminal, It is mounted in the field of another side of the above-mentioned substrate, and has at least one IC die connected to the circuit pattern in the field of another side of the above-mentioned substrate, The power supply terminal provided in this board is connected with the terminal of the first surface state conductor of said capacitor via the circuit pattern linked to the bonding pad for power supplies of said IC die, and the through hole established in said substrate, The earthing terminal formed in this substrate is the semiconductor device connected with the terminal of the second surface state conductor of said capacitor via the circuit pattern linked to the bonding pad for grounding of said IC die, and the through hole established in said substrate, A large surface state conductor can be formed in the rear face of the capacitor which was piled up and constituted from a surface state conductor on both sides of the dielectric by arranging a terminal and an IC die, It has the operation of carrying out noise absorption with bigger electric capacity than claim 2.

[0011]In the semiconductor device according to any one of claims 1 to 3, the invention of this invention according to claim 4 is a spherical shape, arranges each of the signal input/output terminal, power supply terminal, and earthing terminal which were formed in the substrate in the shape of a lattice, and has the operation of making surface mounting possible.

[0012]In the semiconductor device according to any one of claims 1 to 3, the invention of this invention according to claim 5 is pin geometry, arranges each of the signal input/output terminal, power supply terminal, and earthing terminal which were formed in the substrate in the shape of a lattice, and has the operation of enabling socket mounting.

[0013]In the semiconductor device according to any one of claims 1 to 3, the invention of this invention according to claim 6 forms a capacitor in a substrate by printing, and has the operation of excelling in productive efficiency.

[0014]At least one capacitor which the invention of this invention according to claim 7 was allocated on a substrate and this substrate, and was formed in a part of surface state on both sides of the dielectric with the first which has a terminal, respectively, and the second surface state conductor, It is arranged in piles on this capacitor, The circuit pattern and first at least one power supply terminal which connect two or more first signal input/output terminals, two or more second signal input/output terminals, this first, and the second signal input/output terminal, second at least one power supply terminal, third at least one power supply terminal, this first, and the second and the third power supply terminal. It has a circuit pattern which connects the circuit pattern and first at least one earthing terminal to connect, second at least one earthing terminal, third at least one earthing terminal, this first, and the second and the third earthing terminal, It has the TAB package which mounted the IC die which has two or more bonding pads for signal input and output, at least one bonding pad for power supplies, and at least one bonding pad for grounding in this at least one opening of the carrier film which has an opening, The second signal input/output terminal provided in this carrier film is connected to the bonding pad for signal input and output of said IC die, The second power supply terminal provided in this carrier film is connected to the bonding pad for power supplies of said IC die, The

second earthing terminal formed in this carrier film is connected to the bonding pad for grounding of said IC die, Are the semiconductor device which connected with the terminal of said first surface state conductor the third power supply terminal provided in this carrier film, and connected the third earthing terminal with the terminal of said second surface state conductor, and carry out noise absorption with big electric capacity, and. It has the operation that the zone of signal wiring is large, with wiring of microstrip structure.

[0015]In the semiconductor device according to claim 7, the invention of this invention according to claim 8 makes plate shape each of the first signal input/output terminal, the first power supply terminal, and the first earthing terminal, and has the operation of making surface mounting possible.

[0016]In the semiconductor device according to claim 7, the invention of this invention according to claim 9 is a spherical shape, arranges each of the first signal input/output terminal, the first power supply terminal, and the first earthing terminal in the shape of a lattice, and has the operation of making Ogata surface mounting possible.

[0017]In the semiconductor device according to claim 7, the invention of this invention according to claim 10 is pin geometry, arranges each of the first signal input/output terminal, the first power supply terminal, and the first earthing terminal in the shape of a lattice, and has the operation of enabling socket mounting.

[0018]The substrate with which the invention of this invention according to claim 11 was reinforced by the back up plate, At least one capacitor which it was allocated on this substrate and formed in a part of surface state on both sides of the dielectric with the first which has a terminal, respectively, and the second surface state conductor, It is arranged in piles on this capacitor, The circuit pattern and first at least one power supply terminal which connect two or more first signal input/output terminals, two or more second signal input/output terminals, this first, and the second signal input/output terminal, second at least one power supply terminal, third at least one power supply terminal, this first, and the second and the third power supply terminal. It has a circuit pattern which connects the circuit pattern and first at least one earthing terminal to connect, second at least one earthing terminal, third at least one earthing terminal, this first, and the second and the third earthing terminal, It has the TAB package which mounted the IC die which has two or more bonding pads for signal input and output, at least one bonding pad for power supplies, and at least one bonding pad for grounding in this at least one opening of the carrier film which has an opening, The second signal input/output terminal provided in this carrier film is connected to the bonding pad for signal input and output of said IC die, The second power supply terminal provided in this carrier film is connected to the bonding pad for power supplies of said IC die, The second earthing terminal formed in this carrier film is connected to the bonding pad for grounding of said IC die, The third power supply terminal provided in this carrier film is connected with the terminal of said first surface state conductor, The third earthing terminal is connected with the terminal of said second surface state conductor, and it is a semiconductor device arranged on both sides of the capacitor allocated in said substrate with said back up plate and said TAB package, and has the operation that shape is stable.

[0019]In the semiconductor device according to claim 11, the invention of this invention according to claim 12 uses the back up plate as metal, and has the operation of excelling in heat dissipation nature.

[0020]In the semiconductor device according to claim 11, the invention of this invention

according to claim 13 carries out alumite treatment of the surface of this aluminum, and has the operation of excelling in heat dissipation nature while it makes the back up plate aluminum.

[0021]In the semiconductor device according to claim 11, the invention of this invention according to claim 14 prints and forms a capacitor in the back up plate, and has the operation of excelling in productive efficiency.

[0022]Drawing 1 is a sectional view of the pin grid array form package by a 1st embodiment of this invention. In drawing 1, 25 is a substrate, 26 is an IC die, and 27 is a signal input/output terminal (in this embodiment, for convenience). it is called a signal input/output terminal including a signal input terminal, a signal output terminal, and a signal input/output terminal -- it is -- 28 is a power supply terminal, 29 is an earthing terminal and the terminals 27, 28, and 29 are carrying out pin geometry, respectively. 30 is the first surface state conductor, 31 is the second surface state conductor, and 32 is a dielectric and forms the capacitor on both sides of the dielectric 32 for a start between the second surface state conductor 30 and 31. 33 is the vamp as a bonding pad provided in IC die 26, 34 is an insulating layer, and 35 is a circuit pattern.

[0023]The substrate 25 forms resin materials, such as ceramics, glass, and epoxy, in tabular, and the insulating layer 34 forms organic system insulating materials, such as epoxy, a miler, and polyimide, by printing etc. When resin materials, such as epoxy, are used for the substrate 25, the circuit pattern 35 etches the laminated circuit board which laminated this substrate material and copper foil, and is formed. What [otherwise printed the electric conduction ink in which the circuit pattern 35 kneaded silver and copper], What [printed the electric conduction ink in which it formed by vacuum evaporation, weld slag, etc., and the first and second surface state conductors 30 and 31 kneaded silver and copper], Forming by vacuum evaporation, weld slag, etc., the dielectric 32 prints and forms inorganic materials, such as organic materials, such as epoxy, a miler, and polyimide, barium titanate, lead titanate.

[0024]The substrate 25 with which the semiconductor device of this example has two or more signal input/output terminals 27, at least one power supply terminal 28, and at least one earthing terminal 29, Surface mounting is carried out to this substrate 25, At least one IC die 26 which has two or more bonding pads 26-1 for signal input and output and at least one bonding pad 26-2 for power supplies which were connected to the circuit pattern 35 provided in the above-mentioned substrate, respectively, and at least one bonding pad 26-3 for grounding, It has the capacitor which was formed on both sides of the dielectric 32 with first at least one surface state conductor 30 and the second surface state conductor 31, and was allocated by the above-mentioned substrate 25 via the insulating layer 34. Said first surface state conductor 30 and the second surface state conductor 31 provide terminal 30-1,31-1 in a part of surface state, respectively, The bonding pad 26-2 for power supplies of said IC die was connected with said power supply terminal 28 and the terminal 30-1 of said first surface state conductor, and the bonding pad 26-3 for grounding of said IC die, the terminal 31-1 of said second surface state conductor, and said earthing terminal 29 are connected.

[0025]Thus, the terminal 30-1 of the first surface state conductor 30 of the capacitor which was piled up and constituted from the surface state conductors 30 and 31 on both sides of the dielectric 32 is connected to the circuit pattern which connects the power supply terminal 28 and the bonding pad 26-2 for power supplies of an IC die, The terminal 31-1

of the second surface state conductor 3 of said capacitor is connected to the circuit pattern which connects the earthing terminal 29 and the bonding pad 26-3 for grounding of an IC die, and it is considered as a bypass capacitor. Therefore, the high frequency noise superimposed on power supply voltage can be made to bypass near the IC die.
[0026]Since a capacitor can be formed in the substrate face of a large area instead of the IC-die circuit formation side top of a narrow area like the conventional example of drawing 7, Arrangement formation of this capacitor can be carried out, respectively between the bypass capacitor of big electric capacity, two or more bonding pads for power supplies, such as a microprocessor, each bonding pad for power supplies of the IC die provided with the bonding pad for grounding, and the bonding pad for grounding.
[0027]Drawing 2 is a sectional view of the ball grid array form package by a 2nd embodiment of this invention. In drawing 2, 26 is an IC die, 27 is a signal input/output terminal, 28 is a power supply terminal, 25 is a substrate and the terminals 27, 28, and 29 are carrying out [29 is an earthing terminal and] the spherical shape, respectively. 30 is the first surface state conductor, 31 is the second surface state conductor, and 32 is a dielectric and constitutes the capacitor on both sides of the dielectric 32 for a start between the second surface state conductor 30 and 31. 33 is the vamp as a bonding pad provided in IC die 26, 35 is a circuit pattern, and 36 is a through hole.
[0028]IC die 26 Many bonding pads 26-1 for signal input and output, It has at least one bonding pad 26-2 for power supplies, and at least one bonding pad 26-3 for grounding, and in drawing 2, after the vamp 33 is formed in each bonding pad, face down bonding is carried out to the substrate 25.
[0029]It forms in the free space of the circuit pattern 35 which formed the capacitor on both sides of the dielectric 32 with the first surface state conductor 30 and the second surface state conductor 31, and was formed in the substrate 25, and the terminals 27, 28, and 29 mounted in the rear face which mounted IC die 26.
[0030]The substrate 25 provided with two or more through holes 36 where the semiconductor device of this example flows through substrate both sides, At least one IC die 26 by which bonding pad 26-1,26-2 and 26-3 were connected to the circuit pattern 35 which surface mounting was carried out to one field of this board 25, and was provided in the above-mentioned substrate 25, respectively, Two or more signal input/output terminals 27 and at least one power supply terminal 28 which were provided in the field of another side of this board 25, and at least one earthing terminal 29, It is in the field of another side of this substrate 25, was allocated in the free space of these terminals 27, 28, and 29 and the above-mentioned substrate 25 except the through hole 36, and has the capacitor formed on both sides of the dielectric 32 with first at least one surface state conductor 30 and the second surface state conductor 31. Said first and the second surface state conductor 30 and 31 provide terminal 30-1,31-1 in a part of surface state, respectively, The power supply terminal 28 provided in this board 25 connects the through hole 36 established in the first terminal 30-1 and said substrate 25 of the surface state conductor 30, The circuit pattern 35 linked to the bonding pad 26-2 for power supplies of this through hole 36 and said IC die 26 is connected, The earthing terminal 29 formed in this substrate 25 has connected the circuit pattern 35 which connects the through hole 36 established in the second terminal 31-1 and said substrate 25 of the surface state conductor 31, and is connected to the bonding pad 26-3 for grounding of this through hole 36 and said IC die 26.
[0031]Thus, it connects with the through hole 36 which connected the terminal 30-1 of the

first surface state conductor 30 of the capacitor which was piled up and constituted from the surface state conductors 30 and 31 on both sides of the dielectric 32 to the circuit pattern which connects the power supply terminal 28 and the bonding pad 26-2 for power supplies of an IC die, It connects with the through hole 36 which connected the terminal 31-1 of the second surface state conductor 31 of said capacitor to the circuit pattern which connects the earthing terminal 29 and the bonding pad 26-3 for grounding of an IC die, and is considered as a bypass capacitor.

[0032]Therefore, the high frequency noise superimposed on power supply voltage like a 1st embodiment can be made to bypass near the IC die, Arrangement formation of this capacitor can be carried out, respectively between the bypass capacitor of bigger electric capacity than a conventional example, two or more bonding pads for power supplies, each bonding pad for power supplies of the IC die provided with the bonding pad for grounding, and the bonding pad for grounding.

[0033]Drawing 3 is a sectional view of the pin grid array form package by a 3rd embodiment of this invention. In drawing 3, 26 is an IC die, 27 is a signal input/output terminal, 28 is a power supply terminal, 25 is a substrate and the terminals 27, 28, and 29 are carrying out [29 is an earthing terminal and] pin geometry, respectively. 30 is the first surface state conductor, 31 is the second surface state conductor, and 32 is a dielectric and constitutes the capacitor on both sides of the dielectric 32 for a start between the second surface state conductor 30 and 31. 33 is the vamp as a bonding pad provided in IC die 26, 35 is a circuit pattern, and 36 is a through hole.

[0034]IC die 26 Many bonding pads 26-1 for signal input and output, It has at least one bonding pad 26-2 for power supplies, and at least one bonding pad 26-3 for grounding, and in drawing 3, after the vamp 33 is formed in each bonding pad, face down bonding is carried out to the substrate 25.

[0035]It forms in the rear face of the field which mounted the circuit pattern 35, IC die 26, and the terminals 27, 28, and 29 which formed the capacitor on both sides of the dielectric 32 with the first surface state conductor 30 and the second surface state conductor 31, and were formed in the substrate 25.

[0036]The substrate 25 provided with two or more through holes 36 where the semiconductor device of this example flows through substrate both sides, On both sides of the dielectric 32, it is formed in one field of this substrate 25 in the free space except said through hole 36 with first at least one surface state conductor 30 and the second surface state conductor 31, The capacitor which provided terminal 30-1,31-1, respectively in a part of surface state of said first and the second surface state conductor 30 and 31, The signal input/output terminal 27 of plurality [field / of another side of this board 25], at least one power supply terminal 28, and at least one earthing terminal 29, It has the circuit pattern 35 linked to bonding pad 26-1,26-of at least one IC-die 26 and this IC die 26 2, and 26-3. The power supply terminal 28 provided in this board 25 is connected with the terminal 30-1 of the first surface state conductor 30 of said capacitor via the circuit pattern 35 linked to the bonding pad 26-2 for power supplies of said IC die 26, and the through hole 36 established in said substrate 25, The earthing terminal 29 formed in this board 25 is connected with the terminal 31-1 of the second surface state conductor 31 of said capacitor via the circuit pattern 35 linked to the bonding pad 26-3 for grounding of said IC die 26, and the through hole 36 established in said substrate 25, This capacitor can function as a bypass capacitor and the high frequency noise superimposed on power supply voltage like

a 1st embodiment can be made to bypass near the IC die, Since this capacitor can be formed all over the rear face of the field of the substrate 25 which arranged IC die 26, the circuit pattern 35, and the terminals 27, 28, and 29, Arrangement formation of this capacitor can be carried out, respectively between the bypass capacitor of bigger electric capacity than a conventional example, two or more bonding pads for power supplies, each bonding pad for power supplies of the IC die provided with the bonding pad for grounding, and the bonding pad for grounding.

[0037]Drawing 4 is a sectional view of the ball grid array form package by a 4th embodiment of this invention. At least one capacitor which it was allocated on the substrate 25 and this substrate 25, and was formed in a part of surface state on both sides of the dielectric 32 in drawing 4 with the first which has terminal 30-1,31-1, respectively, and the second surface state conductor 30 and 31, It is arranged in piles on this capacitor, Two or more first signal input/output terminals 27-1, two or more second signal input/output terminals 27-2, this first, and the second signal input/output terminal 27-1, 27-2. Circuit pattern 35 and first at least one power supply terminal 28-1, second at least one power supply terminal 28-2, third at least one power supply terminal 28-3, this first, and power supply terminal 28-1,28-of second and ** third 2, and 28-3. [to connect] It has the circuit pattern 35 which connects circuit pattern 35 and first at least one earthing terminal 29-1, second at least one earthing terminal 29-2, third at least one earthing terminal 29-3, this first, and earthing terminal 29-1,29-of second and ** third 2, and 29-3, [to connect] Two or more bonding pads 26-1 for signal input and output. It has the TAB package which mounted IC die 26 which has at least one bonding pad 26-2 for power supplies, and at least one bonding pad 26-3 for grounding in this at least one opening 38 of the carrier film 37 which has the opening 38, The second signal input/output terminal 27-2 provided in this carrier film 37 is connected to the bonding pad 26-1 for signal input and output of said IC die 26, The second power supply terminal 28-2 provided in this carrier film 37 is connected to the bonding pad 26-2 for power supplies of said IC die 26, The second earthing terminal 29-2 formed in this carrier film 37 is connected to the bonding pad 26-3 for grounding of said IC die 26, It connects with the terminal 30-1 of said first surface state conductor 30, and the third power supply terminal 28-3 provided in this carrier film 37 connects the third earthing terminal 29-3 with the terminal 31-1 of said second surface state conductor 31.

[0038]Although the first signal input/output terminal 27-1, first power supply terminal 28-1, and first earthing terminal 29-1 provided in the carrier film 37 are arranged in the shape of a lattice to a field opposite to the field which piled up this capacitor of the carrier film 37 by the spherical shape, respectively and surface mounting is made possible in drawing 4, Pin geometry is used and it is made to perform connector mounting.

[0039]Said capacitor is printed to one field of the substrate 25 in order of the first surface state conductor 30, the dielectric 32, and the second surface state conductor 31, Forming by construction methods, such as weld slag and vacuum evaporation, the substrate 25 has the electric insulation using resin materials whose stock thickness is tens of microns - several millimeters, such as polyimide, epoxy, and phenol, and the thing of the stock thickness beyond abbreviated 1 mm has a function of the back up plate at the time of making superposition connection of the TAB package.

[0040]Since it has connected with the first earthing terminal 29-1, the second surface state conductor 31 and circuit pattern 35 serve as microstrip structure which countered via the

carrier film 37, and the second surface state conductor 31 can extend the zone of the signal passed to the circuit pattern 35 to a high frequency region.

[0041]Drawing 5 is a sectional view of the ball grid array form package by a 5th embodiment of this invention. In drawing 5, it is allocated on the substrate 25 reinforced with the back up plate 39, and this substrate 25, At least one capacitor formed in a part of surface state on both sides of the dielectric 32 with the first which has terminal 30-1,31-1, respectively, and the second surface state conductor 30 and 31, It is arranged in piles on this capacitor, Two or more first signal input/output terminals 27-1. Two or more second signal input/output terminals 27-2. This first and the second signal input/output terminal. Circuit pattern 35 and first at least one power supply terminal 28-1, second at least one power supply terminal 28-2, third at least one power supply terminal 28-3, this first, and power supply terminal 28-1,28-of second and ** third 2, and 28-3. [to connect] It has the circuit pattern 35 which connects circuit pattern 35 and first at least one earthing terminal 29-1, second at least one earthing terminal 29-2, third at least one earthing terminal 29-3, this first, and earthing terminal 29-1,29-of second and ** third 3, and 29-3, [to connect] Two or more bonding pads 26-1 for signal input and output. It has the TAB package which mounted IC die 26 which has at least one bonding pad 26-2 for power supplies, and at least one bonding pad 26-3 for grounding in this at least one opening of the carrier film 37 which has the opening 38, The second signal input/output terminal 27-2 provided in this carrier film 37 is connected to the bonding pad 26-1 for signal input and output of said IC die, The second power supply terminal 28-2 provided in this carrier film 37 is connected to the bonding pad 26-2 for power supplies of said IC die 26, The second earthing terminal 29-2 formed in this carrier film 37 is connected to the bonding pad 26-3 for grounding of said IC die 26, The third power supply terminal 28-3 provided in this carrier film is connected with the terminal 30-1 of said first surface state conductor 30, It connects with the terminal 31-1 of said second surface state conductor 31, and the third earthing terminal 29-3 is arranged on both sides of the capacitor allocated in said substrate 25 with the back up plate 39 and said TAB package.

[0042]In this example, stock thickness uses for the substrate 25 the polyimide film which is an abbreviated number (10 microns - hundreds of microns), The back up plate 39 makes the substrate 25 intervene as an insulating layer using metal plates, such as aluminum and Cu, While terminal 30-1,31-1 of the first surface state conductor 30 and the second surface state conductor 31 prevents the electric short circuit through the back up plate 39 using a metal plate, generation of heat of IC die 26 is made to radiate heat with low thermal resistance.

[0043]The substrate 25 may form resin materials, such as polyimide and epoxy, in the back up plate 39 by construction methods, such as a spin coat, a flow coat, and printing, and when the back up plate 39 is aluminum, an insulating layer can also be realized by an alumite treatment construction method.

[0044]In the above mentioned embodiment, although the capacitor of the layer structure which sandwiched much more dielectric layer with the surface state conductor of two sheets explained, noise absorption of a broadband is more possible by multilayer-structure-izing.

[0045]Although the example of face down bonding explained mounting of the IC die, an intention and effect of this patent are the same also in face up bonding and wire bonding.

[0046]

[Effect of the Invention]According to this invention, the advantageous effect that the noise of a broadband can be absorbed without carrying out variety a large number mounting of the concentrated-constant type capacitor is acquired as mentioned above.

[Brief Description of the Drawings]

[Drawing 1]The sectional view of the pin grid array form package by a 1st embodiment of this invention

[Drawing 2]The sectional view of the ball grid array form package by a 2nd embodiment of this invention

[Drawing 3]The sectional view of the pin grid array form package by a 3rd embodiment of this invention

[Drawing 4]The sectional view of the ball grid array form package by a 4th embodiment of this invention

[Drawing 5]The sectional view of the hole grid array type package which used the metal plate for the substrate by a 5th embodiment of this invention

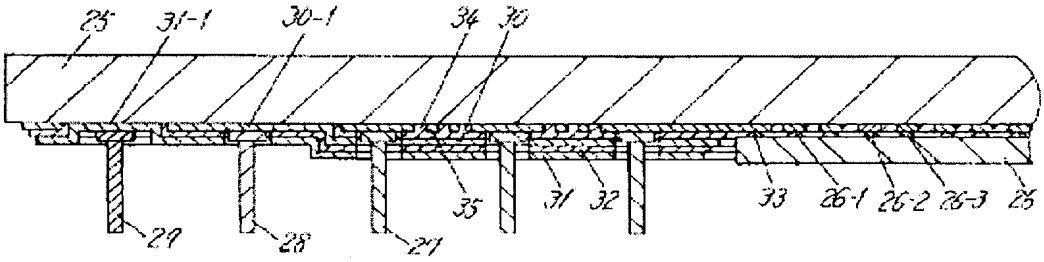
[Drawing 6]The perspective view of the conventional pin grid array form ceramic package for high-speed microprocessors

[Drawing 7]The sectional view of the semiconductor device which carries a capacitor on an IC die

[Description of Notations]

25 Substrate
26 IC die
26-1 The bonding pad for signal input and output
26-2 The bonding pad for power supplies
26-3 The bonding pad for grounding
27 and 27-1,27-2 Signal input/output terminal
28, 28-1,28-2, and 28-3 Power supply terminal
29, 29-1,29-2, and 29-3 Earthing terminal
30 and 31 Surface state conductor
32 Dielectric
33 Vamp
34 Insulating layer
35 Circuit pattern
36 Through hole
37 Carrier film
38 Opening
39 Back up plate

【図１】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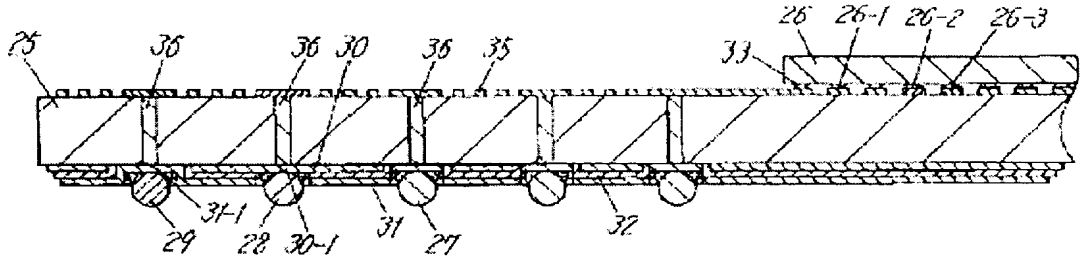
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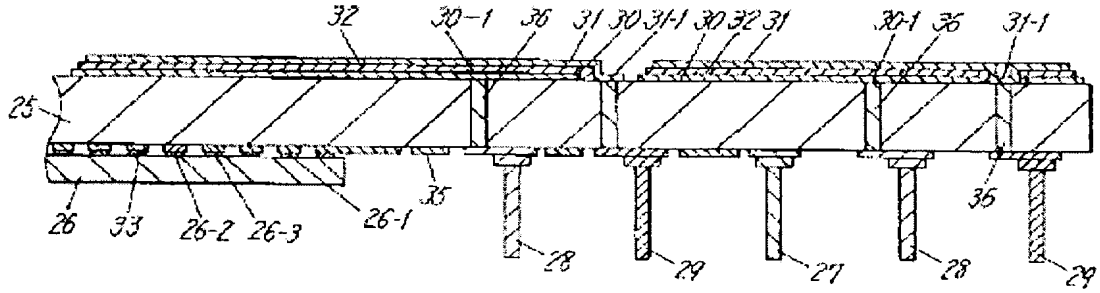
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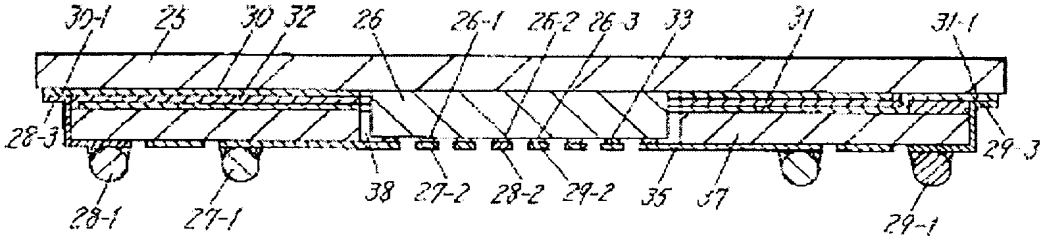
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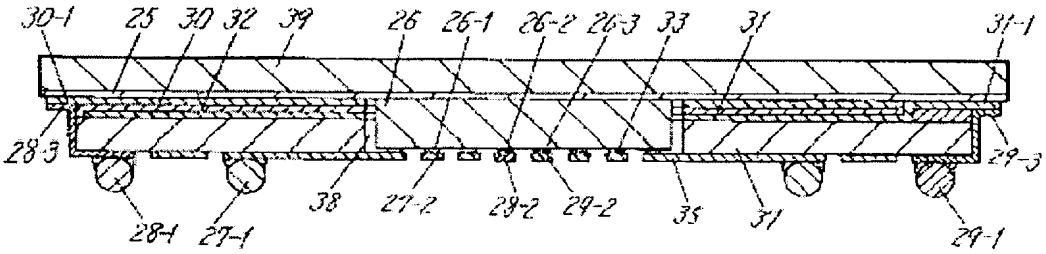
【図５】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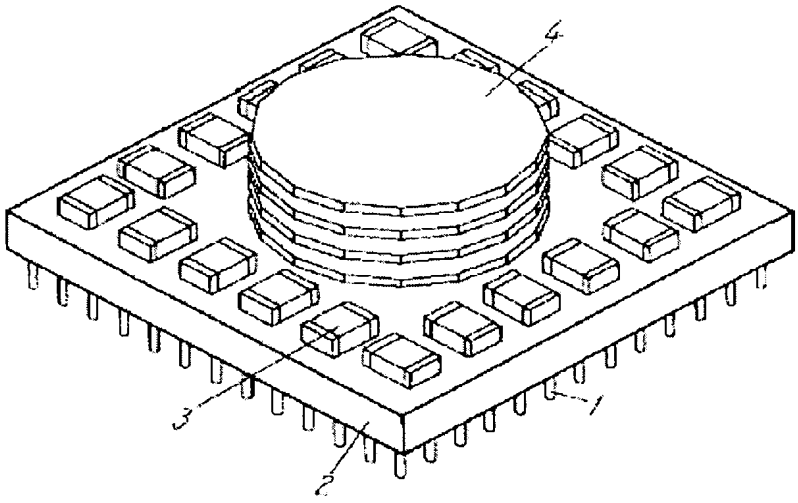
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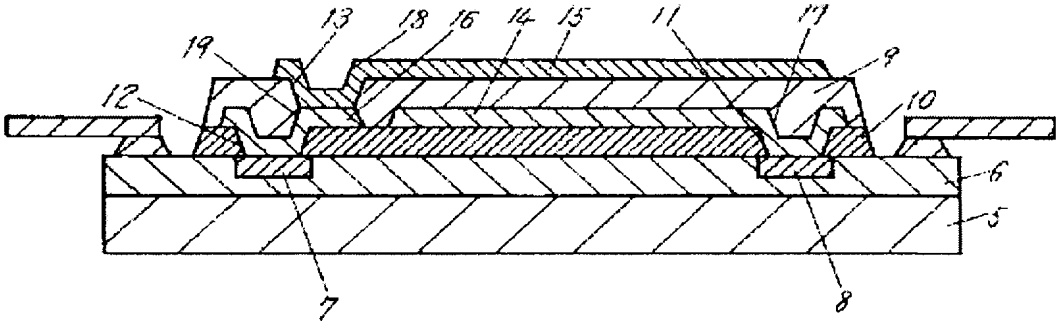
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